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ESTIMATING QUALITY DURING EARLY SYNTHESIS

ABSTRACT OF THE DISCLOSURE

A computer aided system includes a method of improving the accuracy, optimization, and minimization for the synthesis and mapping of logical functions into the logical structures of a target technology, such as the logic cells (e.g., look-up tables) of a 10 programmable logic integrated circuit. In a specific implementation, the invention incorporates late-stage synthesis operations, such as found during a technology mapping operation, into earlier stage synthesis procedures. These late-stage synthesis operations are used to provide better estimates of delay and area of a final compiled design in order to guide optimization operations.

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